



GAU 2811

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PTO/SB/21 (08-00)

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TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	Application Number	09/535,836	
	Filing Date	March 28, 2000	
	First Named Inventor	Hisashi Ohtani	
	Group Art Unit	2811	
	Examiner Name	Hung K. Vu	
Total Number of Pages in This Submission	5	Attorney Docket Number	SEL 173

ENCLOSURES <i>(check all that apply)</i>		
<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Assignment Papers <i>(for an Application)</i>	<input type="checkbox"/> After Allowance Communication to Group
<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
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<input type="checkbox"/> Affidavits/declaration(s)	<input type="checkbox"/> Petition to Convert to a Provisional Application	<input type="checkbox"/> Status Letter
<input type="checkbox"/> Extension of Time Request	<input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address	<input type="checkbox"/> Other Enclosure(s) <i>(please identify below):</i>
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FILE
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4/25/01
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In Re Application of

Ohtani et al.

Serial No.: 09/535,836

Filed: March 28, 2000

For: Semiconductor Device And
The Fabricating Method Thereof

Art Unit: 2811

Examiner: H. Vu

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04/26/2001 53URLES 00000001 501039 09535836 ELECTION AND AMENDMENT A

01 FC:103 216.00 CH
02 FC:102 Sir:60.00 CH

In response to the Restriction Requirement of March 19, 2001, Applicants elect to prosecute Group I: Claims 1-12 and 19-24 in the above-identified application. Applicants are making this election without prejudice to later filing a divisional application on the non-elected claims.

Please also amend the above-identified application as follows:

IN THE CLAIMS:

Please add the following new claims:

Sub
B4
Q1

28. A semiconductor device comprising:

a thin film transistor formed over a substrate, said thin film transistor having a semiconductor layer and a gate electrode adjacent to said semiconductor layer with a gate insulating film interposed therebetween;